IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (Currently Amended) An electronic monitoring circuit provided with an integrated circuit hardware product for assisting a debugger system in debugging an electronic circuit ~~design~~ implemented within the integrated circuit hardware product, said electronic monitoring circuit being ~~automatically~~ created for use with the electronic circuit ~~design~~ and being coupled to the electronic circuit ~~design~~ within the integrated circuit hardware product, said electronic monitoring circuit comprising:

within the integrated circuit hardware product:

a trigger processing unit comprising comparison circuitry for ~~monitoring~~ identifying trigger events and issuing a trigger action based on one or more of the ~~monitored~~ identified trigger events;

~~at least one probe~~ design patching circuitry coupled ~~between the integrated circuit hardware product and said~~ to the trigger processing unit, the design patching circuitry comprising storage circuitry for storing patched values, the design patching circuitry further comprising a multiplexer, the multiplexer having a first input coupled to the storage circuitry and a second input coupled to a patchable signal line within the electronic circuit, the multiplexer having an output coupled to a register, the register having a register output, the register

output to provide the patched values if the first input is enabled, the register output to provide the unpatched values if the second input is enabled;

a configuration register ~~that~~ to stores configuration information for use in configuring ~~said~~ the trigger processing unit ~~or said at least one probe circuit~~; and,

a communication controller ~~operatively~~ ~~connected~~ coupled to ~~said~~ the configuration register to provide external access to ~~said~~ the configuration register by the debugger system.

2. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein ~~at least one probe circuit couples to a region of the electronic circuit design within the integrated circuit hardware product to yield one or more signals for sampling or patching~~the register output is coupled to the storage circuitry so that the patchable signal line is also able to support design visibility.

3. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein said electronic monitoring circuit further comprises:

a status register that stores status information pertaining to the electronic circuit ~~design within the integrated circuit hardware product~~, and

wherein said communication controller is ~~operatively connected~~ coupled to said status register to provide external access to said status register by the debugger system.

4. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein said electronic monitoring circuit further comprises:

an analog-to-digital converter coupled ~~between said at least one probe circuit and~~ to a second signal line within the electronic circuit ~~design within the integrated circuit hardware product~~ and the trigger processing unit, the analog-to-digital converter to provide analog-to-digital conversion from the second signal line to the monitoring circuit.

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5. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein said ~~at least one probe~~ monitoring circuit includes a plurality of probe circuits coupled to signal lines within the electronic circuit and coupled to the trigger processing unit.

6. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein said plurality of probe circuits include at least one of:

a sampling circuit configured to sample at least one of the signals~~; and~~

~~a patching circuit configured to modify at least one of the signals~~ within the electronic circuit.

7. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein a design for said electronic monitoring circuit ~~further being~~ was automatically coupled to a design for the electronic circuit ~~design~~ as part of designing ~~within~~ the integrated circuit hardware product.

8. (Currently amended) An electronic monitoring circuit as recited in claim 1, wherein said electronic monitoring circuit is derived from a HDL description of the electronic circuit ~~design~~.

9. (Currently Amended) An electronic monitoring circuit as recited in claim 1, wherein a design of said electronic monitoring circuit ~~is~~ was automatically created by an instrumentor as part of designing the integrated circuit hardware product.

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10. (Original) An electronic monitoring circuit as recited in claim 1, wherein the monitored trigger events include current trigger events and previous trigger events.

11. (Currently Amended) An electronic monitoring circuit provided with an integrated circuit hardware product for assisting a debugger system in debugging an electronic circuit ~~design~~ implemented within the integrated circuit hardware product, said electronic monitoring circuit being ~~automatically~~ created for use with the electronic circuit ~~design~~ and being coupled to the electronic circuit ~~design~~ within the integrated circuit hardware product, said electronic monitoring circuit comprising:

within the integrated circuit hardware product:

a trigger processing unit comprising comparison circuitry for ~~monitoring~~ identifying trigger events and issuing a trigger action based on one or more of the ~~monitored~~ identified trigger events;

~~at least one probe~~ design patching circuitry coupled ~~between the integrated circuit hardware product and said~~ to the trigger processing unit, the design patching circuitry comprising storage circuitry for storing patched values, the design patching circuitry further comprising a multiplexer, the multiplexer

having a first input coupled to the storage circuitry and a second input coupled to a patchable signal line within the electronic circuit, the multiplexer having an output coupled to a register, the register having a register output, the register output to provide the patched values if the first input is enabled, the register output to provide the unpatched values if the second input is enabled;

a status register ~~that~~ to stores status information pertaining to the electronic circuit ~~design within the integrated circuit hardware product~~; and,

a communication controller ~~operatively connected~~ coupled to ~~said~~ the configuration register to provide external access to ~~said~~ the configuration ~~status~~ register by the debugger system.

12. (Currently Amended) An electronic monitoring circuit as recited in claim 11, wherein ~~at least one probe circuit couples to a region of the electronic circuit design within the integrated circuit hardware product to yield one or more signals for sampling or patching~~the register output is coupled to the storage circuitry so that the patchable signal line is also able to support design visibility.

13. (Currently Amended) An electronic monitoring circuit as recited in claim 11, wherein said electronic monitoring circuit further comprises:

an analog-to-digital converter coupled ~~between said at least one probe circuit and~~ to a second signal line within the electronic circuit ~~design within the integrated circuit hardware product~~ and the trigger processing unit, the analog-to-digital converter to provide analog-to-digital conversion from the second signal line to the monitoring circuit.

14. (Currently Amended) An electronic monitoring circuit as recited in claim 11, wherein said at least one probe circuit includes at least one of:

a sampling circuit configured to sample at least one of the signals~~; and~~

~~a patching circuit configured to modify at least one of the signals~~ within the electronic circuit.

15. (Currently Amended) An electronic monitoring circuit as recited in claim 11, wherein said electronic monitoring circuit is derived from a HDL description of the electronic circuit ~~design~~.

16. (Currently Amended) An electronic monitoring circuit as recited in claim 11, wherein a design of said electronic monitoring circuit ~~is~~ was automatically created by an instrumentor as part of designing the integrated circuit hardware product.

17. (Original) An electronic monitoring circuit as recited in claim 11, wherein the monitored trigger events include current trigger events and previous trigger events.

18. (Currently Amended) An electronic monitoring circuit provided within an integrated circuit hardware product for assisting a debugger system in debugging an electronic circuit ~~design~~ implemented within the integrated circuit hardware product, said electronic monitoring circuit comprising:

within the integrated circuit hardware product:

trigger processing means for monitoring trigger events and issuing a trigger action based on one or more of the monitored trigger events;

at least one probe means for ~~monitoring~~ patching at least one signal of the electronic circuit ~~design~~ within the integrated circuit hardware product; and

communication means for providing external access to said electronic monitoring circuit by the debugger system.

19. (Original) An electronic monitoring circuit as recited in claim 18, wherein said electronic monitoring circuit further comprises:

configuration means for storing configuration information for use in configuring said trigger processing means or said at least one probe means.

20. (Original) An electronic monitoring circuit as recited in claim 19, wherein said communication means provides external access to said configuration means.

21. (Currently Amended) An electronic monitoring circuit as recited in claim 18, wherein said electronic monitoring circuit further comprises:

status register means for storing status information pertaining to the electronic circuit design ~~within the integrated circuit hardware product~~.

22. (Original) An electronic monitoring circuit as recited in claim 21, wherein said communication means provides external access to said status register means.

23. (Currently Amended) An electronic monitoring circuit as recited in claim 18, wherein said electronic monitoring circuit is derived from a high-level HDL description of the electronic circuit ~~design~~.

24. (Original) An electronic monitoring circuit as recited in claim 18, wherein the monitored trigger events include current trigger events and previous trigger events.

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25. (Currently Amended) An integrated circuit product, comprising:

circuitry that implements functionality of said integrated circuit product; and,

customized instrumentation circuitry comprising:

probes inserted into said circuitry that enables a first group of internal signals produced by said circuitry to be examined; and/~~or modified~~,

a signal path that flows from storage circuitry into a signal line of said circuitry, said storage circuitry to store patching values, said signal path and storage circuitry to enable an internal signal produced by said circuitry to be patched on said signal line with said patching values.

26. (Currently Amended) An integrated circuit product as recited in claim 25, wherein said circuitry includes analog and digital portions, and

wherein said customized instrumentation circuitry includes an analog-to-digital converter inserted into said circuitry to enables an internal signals produced in ~~either the~~ an analog ~~or digital~~ portions of said circuitry to be monitored ~~or patched~~.

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27. (Currently Amended) An integrated circuit product as recited in claim 25, wherein ~~said circuitry includes an electronic design, and~~

wherein said customized instrumentation circuitry is customized based on the electronic design associated with said circuitry.

28. (Currently Amended) An integrated circuit product as recited in claim 25, ~~wherein said circuitry includes an electronic design, and~~

wherein said customized instrumentation circuitry is customized based on a user's desired scope of coverage and the electronic design associated with said circuitry.

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29. (New) An apparatus, comprising:

monitoring circuitry within an integrated circuit, said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine, said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register, said monitoring circuitry comprising:

a) a communication link to communicate with said debugger system;

b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said

trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to said output of said register, said comparison circuitry to generate said trigger signal; and,

c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit, said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal.

30. (New) The apparatus of claim 29 wherein said register and said trigger register are designed to receive the same clock signal.

31. (New) The apparatus of claim 29 wherein said monitoring circuitry further comprises:

d) a communication controller coupled to said trigger register and said communication link.

32. (New) The apparatus of claim 29 wherein said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1".

33. (New) The apparatus of claim 29 wherein said register and said trigger register are both n bits wide.

34. (New) The apparatus of claim 29 wherein said ~~manufactured instance of an~~ electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second register and an input of said second register, said monitoring circuitry further comprising:

a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second finite state machine, said second comparison circuitry having a first input coupled to an output of said second trigger register and a second input coupled to said output of said second register, said second comparison circuitry to generate a second trigger signal if said second finite state machine reaches said looked for state of said second finite state machine; and,

second sample circuitry inserted into said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

35. (New) The apparatus of claim 29 wherein said monitoring circuitry was derived from an HDL description of said electronic circuit as part of said integrated circuit's design process.

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36. (New) An apparatus, comprising:

monitoring circuitry within an integrated circuit, said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said integrated circuit, said electronic circuit comprising a finite state machine, said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register, said monitoring circuitry comprising:

a) a communication link to communicate with said debugger system;

b) a trigger processing unit to provide a trigger signal if said finite state machine performs a looked for state transition, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state transition, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to both said finite state machine's combinatorial logic and said output

of said register, said comparison circuitry to generate said trigger signal; and,

c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit, said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal.

37. (New) The apparatus of claim 36 where said looked for state transition comprises an input to said finite state machine's combinatorial logic and an output provided at said register in response thereto, said second input of said comparison circuitry coupled to an input to said finite state machine that is received by said finite state machine's combinatorial logic.

38. (New) The apparatus of claim 36 wherein said register and said trigger register are designed to receive the same clock signal.

39. (New) The apparatus of claim 36 wherein said monitoring circuitry further comprises:

d) a communication controller coupled to said trigger register and said communication link.

40. (New) The apparatus of claim 36 wherein said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1" when defining the finite state machine state register output of said looked for state transition.

41. (New) The apparatus of claim 36 wherein said register and said trigger register are both o bits wide, where o = n + m, and where n is the bit width of said register and m is the number of bits that said comparison circuitry receives from its coupling to said combinatorial logic.

42. (New) The apparatus of claim 36 wherein said electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second register and an input of said second register, said monitoring circuitry further comprising:

a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second finite state machine, said second comparison circuitry having a first input coupled to an output of said second trigger register and a second input coupled to said output of said second register, said second comparison circuitry to

generate a second trigger signal if said second finite state machine reaches said looked for state of said second finite state machine; and,

second sample circuitry inserted into said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

43. (New) The apparatus of claim 36 wherein said electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second register and an input of said second register, said monitoring circuitry further comprising:

a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second finite state machine, said second comparison circuitry having a first input coupled to said second combinatorial logic and an output of said second register, said comparison circuitry having a second input coupled to an output of said second trigger register, said second comparison circuitry to generate a second trigger signal if said second finite state machine performs said looked for state transition of said second finite state machine; and,

second sample circuitry inserted into said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

44. (New) The apparatus of claim 43 wherein said looked for state transition of said finite state machine comprises input data provided to said finite state machine's combinatorial logic and an output provided at said register in response thereto, said second input of said comparison circuitry coupled to an input to said finite state machine that is received by said finite state machine's combinatorial logic.

45. (New) The apparatus of claim 44 wherein said looked for state transition of said second finite state machine comprises input data provided to said second finite state machine's combinatorial logic and an output provided at said second register in response thereto, said second input of said second comparison circuitry coupled to an input to said second finite state machine that is received by said second combinatorial logic.

46. (New) An apparatus, comprising:

monitoring circuitry within an electronic system, said electronic system comprising electronic components, said monitoring circuitry to assist a

debugger system in debugging an electronic circuit implemented within said electronic system, said electronic circuit comprising a finite state machine, said finite state machine comprising combinatorial logic coupled between an output of a register and an input of said register, said monitoring circuitry comprising:

a) a communication link to communicate with said debugger system;

b) a trigger processing unit to provide a trigger signal if said finite state machine reaches a looked for state, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to said output of said register, said comparison circuitry to generate said trigger signal; and,

c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit, said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal.

47. (New) The apparatus of claim 46 wherein said register and said trigger register are designed to receive the same clock signal.

48. (New) The apparatus of claim 46 wherein said monitoring circuitry further comprises:

d) a communication controller coupled to said trigger register and said communication link.

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49. (New) The apparatus of claim 46 wherein said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1".

50. (New) The apparatus of claim 46 wherein said register and said trigger register are both n bits wide.

51. (New) The apparatus of claim 46 wherein said electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second register and an input of said second register, said monitoring circuitry further comprising:

a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second

finite state machine, said second comparison circuitry having a first input coupled to an output of said second trigger register and a second input coupled to said output of said second register, said second comparison circuitry to generate a second trigger signal if said second finite state machine reaches said looked for state of said second finite state machine; and,

second sample circuitry inserted into said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

52. (New) The apparatus of claim 46 wherein said monitoring circuitry was derived from an HDL description of said electronic circuit as part of said electronic system's design process.

53. (New) An apparatus, comprising:

monitoring circuitry within an electronic system, said electronic system comprising electronic components, said monitoring circuitry to assist a debugger system in debugging an electronic circuit implemented within said electronic system, said electronic circuit comprising a finite state machine, said finite state machine comprising combinatorial logic coupled

between an output of a register and an input of said register, said monitoring circuitry comprising:

a) a communication link to communicate with said debugger system;

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b) a trigger processing unit to provide a trigger signal if said finite state machine performs a looked for state transition, said trigger processing unit comprising a trigger register and comparison circuitry, said trigger register to be set by said debugger system through said communication link to define said looked for state transition, said comparison circuitry having a first input coupled to an output of said trigger register and a second input coupled to both said finite state machine's combinatorial logic and said output of said register, said comparison circuitry to generate said trigger signal; and,

c) sample circuitry inserted into said electronic circuit, said sample circuitry coupled to said trigger processing unit, said sample circuitry to sample a signal within said electronic circuit in response to said trigger signal.

54. (New) The apparatus of claim 53 where said looked for state transition comprises an input to said finite state machine's combinatorial logic and an output provided at said register in response thereto, said second input of said

comparison circuitry coupled to an input to said finite state machine that is received by said finite state machine's combinatorial logic.

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55. (New) The apparatus of claim 53 wherein said register and said trigger register are designed to receive the same clock signal.

56. (New) The apparatus of claim 53 wherein said monitoring circuitry further comprises:

d) a communication controller coupled to said trigger register and said communication link.

57. (New) The apparatus of claim 53 wherein said finite state machine is a one hot encoded finite state machine and said trigger register is set by setting a single bit in said trigger register to a logical "1" when defining the finite state machine state register output of said looked for state transition.

58. (New) The apparatus of claim 53 wherein said register and said trigger register are both o bits wide, where o = n + m, and where n is the bit width of said register and m is the number of bits that said comparison circuitry receives from its coupling to said combinatorial logic.

59. (New) The apparatus of claim 53 wherein said electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second register and an input of said second register, said monitoring circuitry further comprising:

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a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second finite state machine, said second comparison circuitry having a first input coupled to an output of said second trigger register and a second input coupled to said output of said second register, said second comparison circuitry to generate a second trigger signal if said second finite state machine reaches said looked for state of said second finite state machine; and,

second sample circuitry inserted into said said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

60. (New) The apparatus of claim 53 wherein said electronic circuit further comprises a second finite state machine, said second finite state machine comprising second combinatorial logic coupled between an output of a second

register and an input of said second register, said monitoring circuitry further comprising:

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a second trigger register and second comparison circuitry, said second trigger register to be set by said debugger system through said communication link to define a looked for state of said second finite state machine, said second comparison circuitry having a first input coupled to said second combinatorial logic and an output of said second register, said comparison circuitry having a second input coupled to an output of said second trigger register, said second comparison circuitry to generate a second trigger signal if said second finite state machine performs said looked for state transition of said second finite state machine; and,

second sample circuitry inserted into said electronic circuit, said second sample circuitry coupled to second comparison circuitry, said second sample circuitry to sample another signal within said electronic circuit in response to said second trigger signal.

61. (New) The apparatus of claim 60 wherein said looked for state transition of said finite state machine comprises input data provided to said finite state machine's combinatorial logic and an output provided at said register in response thereto, said second input of said comparison circuitry coupled to an input to said

finite state machine that is received by said finite state machine's combinatorial logic.

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62. (New) The apparatus of claim 61 wherein said looked for state transition of said second finite state machine comprises input data provided to said second finite state machine's combinatorial logic and an output provided at said second register in response thereto, said second input of said second comparison circuitry coupled to an input to said second finite state machine that is received by said second combinatorial logic.

COMMENTS

The enclosed is responsive to the Examiner's Office action mailed on November 6, 2003. At the time the Examiner mailed the Office Action claim 1 – 28 were pending. By way of the present response the Applicants have: 1) amended claims 1-9,11-16,18, 21, 23 and 25-28; and, 2) added new claims 29 - 62. As such claim 1-62 are currently pending. The Applicants respectfully request reconsideration of the present application and the allowance of claims 1-62.

Independent claims 1, 11, 18 and 25 stand rejected under 35 USC 102(b) as being anticipated by the Dervisoglu reference. However, the Examiner indicated that dependent claims 6 and 14 would be allowable if rewritten into independent form. Each of dependent claims 6 and 14 are directed, at least in part, to design patching. Therefore the Applicants have amended each of independent claims 1, 11, 18 and 25 to incorporate elements directed to design patching. Design patching is discussed at least in reference to Figure 9 of the Applicant's specification.

The Applicants respectfully submit that the Dervisoglu reference (as well as the other references cited by the Examiner) fails to disclose, teach or suggest matted directed to design patching and that each of independent claims 1, 11, 18 and 25 are presently in allowable form. Therefore the Applicants respectfully request the allowance of all claims.

New claims 29 – 62 are directed to triggering through finite state machine state detection and finite state machine state transition detection. The Examiner is directed to Figures 8, 11 and 12 and related discussions within the Applicants' specification for support of new clams 29 - 62. The Dervisoglu reference appears to contain no teaching of triggering through finite state machine state detection and finite state machine state transition detection. Therefore, the Applicants respectfully submit that new claims 29 –62 are patentable over the Dervisoglu reference.